USC Viterbi
School of Engineering
Ming Hsieh Department of Electrical and Computer Engineering

Ming Hsieh Institute **Seminar Series**

Integrated Systems

Recent Trends and Advances in High Performance Fractional-N PLL Design

Dr. Wanghua Wu

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Date: Friday, September 30th, 2022 - Time: 2:00pm -Location: EEB 132
Zoom Link/Code: Meeting ID: 926 7347 1681, Passcode: 960345
Refreshments will be served

Abstract: High performance fractional-N phase-locked loops (PLLs) are essential elements of any advanced electronic systems. In recent years, both analog and all-digital PLLs employing sampling or sub-sampling phase detector have gained popularity and demonstrated below 100-fs integrated jitter and superior figure-of-merit. This talk focuses on this PLL architecture and elaborates the advanced design techniques to achieve low jitter, low fractional spurs, fast locking, and low power operation. Both circuit design and digital calibration techniques will be presented in detail. In addition, recent advances in reference clock generation will also be discussed as it is crucial for high performance PLLs.

Biography:

Dr. Wanghua Wu received the B.Sc. degree from Fudan University, Shanghai, China, in 2004, M.Sc. degree and Ph.D. degree from Delft University of Technology, The Netherlands in 2007 and 2013, respectively, all in electrical engineering. From 2013 to 2016, she was an RFIC Design Engineer in Marvell, developing high-performance frequency synthesizers for WLAN transceivers. Since 2016, she has been with Samsung Semiconductor Inc. USA. She is currently a Principal Engineer and Senior Manager, leading advanced cellular RFIC design. Her research interest is on CMOS frequency synthesis for wireless applications. She currently serves as the Technical Program Committee member of IEEE International Solid-State Circuits Conference (ISSCC), Custom Integrated Circuits Conference (CICC), and Radio Frequency Integrated Circuits Symposium (RFIC).

Hosted by Prof. Hossein Hashemi, Prof. Mike Chen and Prof. Constantine Sideris
Organized and hosted by Vinay Chenna (vchenna@usc.edu).